The Regulator/Audio PCB has the dual function of regulating the +5 VDC logic power to the game PCB and amplifying the audio from the game PCB.

Regulator Circuit

The regulator consists of voltage regulator Q1, Q2, Q3, and Q4. A source power transistor Q3 and Q4 is used to provide power to the game PCB by monitoring the voltage through the source enable inputs +VSENSE and -VSENSE. The regulator directly supplies power to the +5 VDC and ground inputs to the game PCB. The regulator regulates the voltage at the +5 VDC and ground inputs to the game PCB. This eliminates a reduced voltage drop built-up on the wire harness between the regulator and the game PCB. Variable resistor R9 is adjusted for the voltage at the +5 VDC and ground inputs to the game PCB. Once adjusted, the voltage at the +5 VDC and ground inputs to the game PCB will remain constant at this voltage.

Regulator Adjustment

1. Connect a voltmeter between +5 V and GND test point of the game PCB.
2. Adjust variable resistor R9 on the Regulator/Audio PCB for +5 V reading on the voltmeter.
3. Connect a voltmeter between +5 V REG and GND test point of the Regulator/Audio PCB. Voltage reading shall be greater than +5.5 VDC. If greater, try cleaning connectors on both the game PCB and Regulator/Audio PCB.
4. If cleaning in step 3 above does not return voltage below +5.5 VDC, connect the GND test point of the Regulator/Audio PCB and plus GND test point of the game PCB. Note the voltage drop, then connect minus lead of voltmeter to +5 V REG test point on Regulator/Audio PCB and plus lead to +5 VDC test point on game PCB. From this you can estimate the appropriate harness wire or harness connector.

Audio Circuit

The audio circuit contains two independent amplifiers. Each amplifier consists of a TDA amplifier with a gain of ten. In Asteroids, the DISABLE input to the PCB is permanently grounded. Therefore, the audio circuit is always on, even when the game is in the attract mode.

The audio circuit is repeated on Sheet 2, Side B, in more detail.
CLOCK CIRCUIT

The clock circuit consists of crystal XV and associated inverters and counters C4 and C5. Counters C4 and C5 count the crystal frequency down to the frequencies necessary for the Asteroids game.

POWER RESET AND WATCHDOG COUNTER

During initial power-up, the delayed charging of capacitor C26 causes a preset of flip-flop C4 and a clear of counter C5. This results in holding RESET input to the MPU high. When the charge of C26 reaches about 1.5 VDC, preset and clear inputs are removed. Counter C5 counts to 128 at 3 KHz rate and RESET is removed (drops high) from the input of the MPU. This allows the logic power input to the PCB to stabilize before allowing the MPU to begin its initialization routine.

If the MPU program is operating properly, the MPU address decoding circuitry will output the WDCDR (Watchdog clear) signal at predetermined intervals. This serves to clear counter C5 before it counts up to the state that will create the RESET condition. If the MPU program stays from its intended sequence and does not output the WDCDR signal, counter C5 will count up to the RESET state and cause the MPU to return to its initialization routine.

NMI COUNTER

The Nmi (non-maskable interrupt) counter causes an interrupt at the NMI input of the MPU every 4 mcs. The interrupt is derived by dividing 3 KHz by a factor of 12 through counter C5. The interrupt occurs when pin 9 of integrated circuit B5 goes low. During power-up, the NMI counter is disabled by RESET. During Self-Test, the NMI is disabled by TEST.

POWER INPUT

This circuitry consists of the PCB input and outputs for the +5 VDC logic power and 36 VAC input to the on board regulator. The +5 VDC inputs and outputs are discussed on Sheet 1, Side A of this schematic set.

The 36 VAC inputs are received by two full wave rectifiers. Diodos C10 and C11 rectify the negative pulse of the input and the 7815 regulates the voltage at +15 VDC. Diodos C12 and C13 rectify the positive pulse of the 36 VAC input and the 7815 regulates the voltage at +15 VDC. The 7812 regulates at +12 VDC. The 7805 regulates an additional +5 VDC for the DACs. Zener diode CR4 supplies the +8.2 VDC for the sample and hold circuit. The +12V (unregulated) is used to power operational amplifiers PA1 and PA2 in the audio output.

FROM SWITCH INPUTS SHEET 2, SIDE B

ROM/PROM CIRCUITRY

Program Memory for the Asteroids is contained in PROMs for the 60 version ROMs for the 42 version of the PCB equivalent to four PROMs -2 PROMs a common enable must be removed with a ROM. For example, remove locations F2, H1, L2 and L1 before ROM at location F1.
MPU CIRCUITRY

NOTE: DO NOT USE SPLIT PADS ON PCB FOR TROUBLESHOOTING PURPOSES.

ADDRESS DECODING CIRCUITRY

The address decoder performs the function of turning on or enabling the appropriate circuitry at the critical time, so that information can be transferred back and forth between the game circuitry and the MPU. The memory map below is for the Asteroids game.

If you are going to use the Automatic RAM-ROM Tester, please remember to remove MPU C3 and ground the WOOG DISABLE test point.

Asteroids game is a version of the PCB or the PCB. One ROM is (ROMs) connected to removed before replacing, remove PROMs at before replacing with.

RAM CIRCUITRY

The RAM is the temporary storage space for the MPU and is enabled when ZP (Zero Page) is enabled. When Vنان from the MPU is low, the RAM stores the data byte input to the MPU at the location addressed by the MPU address bus (0B0 to 0B7). When Vنان is high, the MPU reads the stored data byte at the addressed location.

The signal RAMSEL, when low, has the effect of swapping pages 2 and 3 within the RAM. This allows greater programming flexibility.

Memory Components and Their Equivalents (Locations Shown in Bold)

-01 P.C. Boards
(PROMs)
Alternate 01 P.C. Boards
(PROMs)
-02 P.C. Boards
(ROMs)

035131-01 J2
035150-01 J2
035143-01 C1
035132-01 N2
035151-01 N1
035153-01 H1
035134-01 M2
035158-01 J1
035140-01 M1
035150-01 F2
035152-01 L2
035143-01 M1
035142-01 L1
VECTOR GENERATOR PROGRAM COUNTER

Counts F5, H6 and J6 contain the address of the next data byte (instruction) to be fetched from the Vector Generator memory. Because these counters point to the next instruction in memory to be retrieved and performed, they are called the program counter. This program counter is incremented by one count (to data latches F7 and H7 and buffers H6 and J6). The program counter may also be preset to "jump" to a new address. This new address can be loaded into the program counter from the vector generator memory via data latches F7 and H7 and buffers H6 and J6. The program counter may also be preset to "return" to a previous address which B6 unless the microcomputer is addressing the ROM data via Timer 0 and 8 and decode the memory address. This address consists of registers F4, H4, J4, and K3. The stack is a 4-word (128-bit) memory, used to save the contents of the program counter for future reference. When the stack is low, it is loaded with the memory address via the input data bus. Immediately after information is written into the stack, counter K3 increments one count. Immediately before loading the program counter from the stack, counter K3 decrements one count.

VECTOR GENERATOR MEMORY ADDRESS SELECTOR

The address selector consists of multiplexers F3, H3, J3 and K3. When VMEM is low, the MPU of the microcomputer gains access to the address inputs of the vector generator memory. In this state, IF and WR are both low. When VMEM is high, the address input to the vector generator memory is from the vector generator program counter and state machine. In this state, IF and WR are both high. The pull-up resistors connected to the 29 and 36 inputs of multiplexer K3.

Address decoder L3 and address bits A11 and A12, and selects the RAM or one of the ROMs of the vector generator memory.

This address selecting arrangement allows the game MPU to access the vector generator memory, i.e., write data into the vector generator RAM to instruct the vector generator what it should do next. The address selector can then allow the vector generator program counter and state machine to access this same area of RAM also, and read what instructions were sent to it by the game MPU.

STATE MACHINE

The state machine is the "master controller" of the vector generator circuitry. It is the MPU, via the vector generator RAM. It carries out these instructions by accessing the appropriate sections of the vector generator ROM memory, using the vector generator program counter to do so. The state machine reads the vector generator RAM data via Timer 0 and 8 and decodes the memory address. Initially, the state machine reads the vector generator data latches (Timer 0 and 8). This makes Timer 0 and 8 signals low. The state machine now begins executing instructions, starting at vector memory location 0.

The purpose of the vector timer is to time out the length of time it takes to "draw" an entire vector on the monitor display. During the interval when the X and Y position counters are actually drawing a vector, STOP is high. This prevents the vector generator state machine from advancing to its next state until the vector currently being drawn is complete. As soon as the vector has been drawn, STOP goes low, allowing the state machine to advance to the next state in its intended sequence.

The vector timer consists of four multiplexers, F3, decoder E7, LATCH M7, ADDER M6, and counters B7, C7, and D7. M7 contains a scale factor which is added in B7 to the timer signal each time. Timer 0 and 8 inputs are the state signals but all high, decoder E7 directly decodes the sum, and the decoded low into one of the counters. When GO goes low, the counters count the load count until the vector reaches the maximum count. This count is a maximum length of 1024. At the end of the timer cycle, the state machine goes high and clears the GO flip-flop of the state machine.

If the TIMER signals are all high, the vector generator RAM goes low and data signals D11 and D71 are decoded by decoder E7. This is added to the scale factor and loaded into the counters.
The vector generator memory consists of 2K of RAM and 4K of ROM. It may be directly accessed by the MPU through the direct memory access (DMA). Data is written in from the microprocessor to the data buffer when the WRITE input is high.

The 2K x 8 vector generator program memory chip 273955 may be substituted with two equivalent 1K x 8 chips in location A2 and B4.

The 10 x 10 display computed by the microprocessor is stored as a 1024 x 1024 matrix. Each element of the matrix is stored as a 4-bit color value. The matrix is refreshed at 60Hz. The matrix is divided into 16 x 16 sub-matrices, each one of which is stored in a separate 1024 x 1024 matrix. The matrix is refreshed at 60Hz. The matrix is divided into 16 x 16 sub-matrices, each one of which is stored in a separate 1024 x 1024 matrix. The matrix is refreshed at 60Hz.

The data latches consist of latch 0 (A7), latch 1 (A7), latch 2 (A7), and latch 3 (A7). Inputs D0 through D7 are the data inputs from the vector generator memory. Latches 0 through 3 are directly clocked by the rising edge of the clock. Latches 0 and 7 are output by the vector generator and are transferred to the latch of the program memory chip 273955. Latch 3 is cleared when the data latch is high. Latch 0 is not cleared when the data latch is low.Latch 0 is cleared by ALPHANUM.

X and Y Position Counters

The X and Y position counters are used to keep track of the position of the beam on the screen. The counters are reset at the beginning of each frame and increment by one each time the screen is updated. If the count reaches 4095, the counter wraps around to 0.

The counters are implemented using a simple 8-bit counter circuit. The counter is clocked by a 6.25 MHz oscillator. The oscillator is a typical CMOS oscillator circuit that produces a stable clock signal.

The counter is reset at the beginning of each frame by the frame start signal. The frame start signal is generated by the frame counter and is used to trigger the oscillator.

The frame counter is a simple 4-bit counter that is reset at the beginning of each frame. It is clocked by the 100 nsec clock signal from the oscillator. The 100 nsec clock signal is generated by dividing the 6.25 MHz oscillator signal by 64.

The oscillator circuit is shown below. The oscillator is a typical CMOS oscillator circuit that produces a stable clock signal.

The clock signal is used to drive the 8-bit counter. The counter is reset at the beginning of each frame by the frame start signal. The frame start signal is generated by the frame counter and is used to trigger the oscillator.

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PLAYER INPUT CIRCUITRY

DIAG STEP diagnostic steps, 3 KΩ, SEL-TEST SLAM, HALT, FIRE and HYPER inputs are read by the MPU when SHUT (switch input) zero enable is low. Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on DB7. Switch inputs or active when pulled to ground. DIAG STEP, 3 KΩ, and SEL-TEST signals are read into the MPU to initiate and control the play's self-test procedure. SLAM is a signal read by the MPU to indicate the status of the anticlock switch mounted on the coin door. The MPU reads HALT to determine the state of the vector generator.

The coin door and some control panel switches are read by the MPU when SHUT switch input one enable is low. Switches to be read are selected by AB0 thru AB2 from the MPU. All inputs are read on data line DB7. Switch inputs are "on" when pulled to ground.

The game option switches are read by the MPU when OPTION option switch enable is low. Switch toggles to be read are selected by AB0 and A1 from the MPU. Switch toggles 1, 2, 3, 4, 5, and 7 are read on data line DB6 and toggles 2, 4, 6, and 8 are read on DB7. Toggle inputs are "on" when pulled to ground.

The OUTPUT circuitry

The HI AMP sound is heard throughout the game. The HI AMP is connected as an oscillator, enabled by N7 pin 2. The frequency is determined by the current coming out of Q2. This depends on its value, which is derived from the four-bit code in N7.

The SAUCER sound is heard when an enemy saucer appears. The 555 is a voltage-controlled oscillator. Its modulating voltage is derived from the 556. The 556 is a low-frequency oscillator. The effect is a wailing sound. SAUCER-A changes some component values in order to provide for different saucer sounds.

The FIRE sounds for the Saucer and the Space Ships are generated by two identical circuits. Each contains a 555 operating as a voltage-controlled oscillator. The Saucer FIRE sound is initiated by SAUCER-A, and the Space Ship FIRE sound is initiated by SHIP/FIREA. Each of the 555s is configured in such a way that when they are enabled, they output a signal of a specific frequency and amplitude. This signal begins to decay immediately, both in frequency and amplitude, due to the discharge of the control capacitor (C38 & 39 for Saucer FIRE Sound, C47 & 48 for Ship/FIRE Sound).

The EXPLODE sound is heard when any object is sampled at the icon by FIRE and CONTROLLING RATE change in position. The noise is modulated in IF.

The EXPLODE sound is heard when any object is sampled at the icon by FIRE and CONTROLLING RATE change in position. The noise is modulated in IF.

The video inverter circuitry is only used in a cocktail game. In an upright game, pin 19 is unconnected and therefore floats. When pin 19 floats, transistor Q16 is turned off and transistor Q17 is turned on. Therefore, IN is ~82 VDC and NONINV is ~5 VDC. This result is a non-inverted video output. When the video for player 1 is being displayed, pins 1 and 19 are ~5 VDC. This results in a non-inverted video output. When the video for player 2 is being displayed, pins 7 and 19 are grounded. This causes transistor Q16 to be turned on and Q17 to be turned off. Therefore, INV is ~82 VDC and NONINV is ~5 VDC. The result is an inverted X-axis and Y-axis output, killing the monitor's display to be upside down.

R9 and P9 generate random noise. This noise is filtered by P10 and produces the rumble sound heard when the ship is throttling.
AUDIO OUTPUT

All sounds are mixed in 1/4 of P11. This is Audio 1. The signal is then inverted by another 1/4 of P11 and becomes Audio 2. These outputs provide a push-pull output to the audio section of the Regulation/Analog PCB.

LAMP, LED, AND COIN COUNTER OUTPUT

This circuit consists of coin counter drivers Q11, Q12, Q13 and data latch N11, clocked by the microcomputer's address decoder. When the input to a driver is clocked high, its collector goes low, grounding the return of the coin counter in the coin door. When START1 or START2 is clocked low, it grounds the START LEDs in the control panel.

VIDEO OUTPUTS

The video output circuit consists of three individual circuits: X axis, Y axis, and Z axis video output circuits. The X axis and Y axis video output circuits each consist of a digital-to-analog converter (DAC), current-to-voltage converter, two sample and hold, and amplifier. The Z axis video output circuit consists of a shift register and a summer.

X and Y Outputs

The DACs (Q11 and B11) each receive binary numbers from the vector generator's position counters outputs. These numbers represent the location of the beam on the monitor. For the non-inverted X axis, the numbers range from 0 to 1023, all 0 is at the left edge of the monitor screen, 1023 is at the center, and 2048 is at the right edge. For the non-inverted Y axis, the numbers range from 256 to 1023, all 0 is at the bottom of the monitor screen, 1023 is at the center, and 2048 is at the top. When the X axis and Y axis are inverted, the monitor picture is turned upside down. This is used for a two-player cocktail game.

The DACs convert these binary numbers to current outputs. The DACs' current outputs are applied to the pin 6 inputs of current-to-voltage converters C112 and C113. From these current-to-voltage converters, the signal is fed to two sample-and-hold circuits. One is non-inverted and the other is inverted. The non-inverted sample and hold consists of one stage of analog switch D12 and capacitor C168 for the X axis, B16 and C106 for the Y axis. The inverting sample and hold consists of inverter I12, one stage of analog switch D12, and capacitor C119 for the X axis and B112, B112 and C118 for the Y axis.

The sample and hold circuits are controlled by SH/ex (sample and hold control). SH/ex is derived by gating 3 MHz from the microcomputer clock circuitry and VGS (gate-source voltage) of the vector generator's state generator. The result of these inputs ensures that the non-inverted or inverted analog signals that are applied to the analog switches are sufficiently stabilized before being applied to the sample and hold capacitors.

The output swing of SH/ex is ±8 to ±8 VDC. When SH/ex is high, the voltage gain is selected to be the same as the analog switch. These switches select the non-inverted or inverted X axis and Y axis outputs. The output is then amplified by the second stage of C12 and C12 for an impedance-matched output to the X and Y inputs to the monitor. Since the monitor does not have adjustable X and Y gains, the gains are adjustable by variable resistors R130 and R132.

Z Output

The Z axis video output receives six inputs. BVL/D (beam valid), from the output of the vector generator's position counters, tells the Z axis to draw the line. BLANK (blanks line), from the vector generator's state machine, tells the Z axis to stop drawing a line. SCALE0 through SCALE3 (gray level shading) are inputs from the output of vector generator's data latch. This is the Z axis gray level shading of the line that is being drawn on the monitor.

When BVL/D and BLANK are both high, a high is clocked through flip-flop K9 that turns transistor Q3 on. This allows the scale inputs to be passed through transistor Q2. When BLANK goes low, a low is clocked through K9, transistor Q3 turns on, and the signal is grounded at the base of transistor Q2.

The scale inputs are applied to the base of transistor Q11 determine Q11's emitter voltage, during the line draw period. The SCALE 0 through SCALE3 resistors R36 through R55, resistor R65, and resistor R66 result in a range of about +1.0 to -1.0 VDC when all inputs are high. The emitter of Q11 follows at about +1.0 to +1.0 VDC, while the emitter of transistor Q21 follows at about +1.0 VDC. This output is applied to the Z input of the monitor. Since there is brightness and contrast control in the monitor, there are no adjustments in this circuit.

Sheet 2, Side B

ASTEROIDS Switch Inputs, Coin Counter, LED and Audio Outputs

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